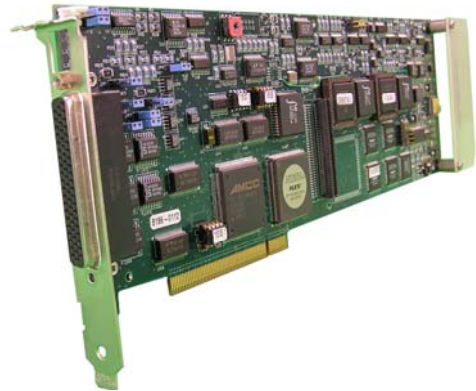


## PCI-based PCM Bit Synchronizer Board TSNCxx-400

### Features

- IRIG PCM Formats
- Selectable Loop Bandwidths
- BER Performance Better than 1.0 dB
- Complete Programming Documentation and Stand-alone Setup Software
- Optional Convolutional (Viterbi) Decoder and Deinterleaver
- Built-in Self-test Pattern Generator
- Optional Support for QPSK PCM Streams
- Optional On-board Simulator
- Tunable Bit Rates Up to 40 Mbps
- Occupies Single PCI Slot
- Selectable PCM Output Codes



### Introduction

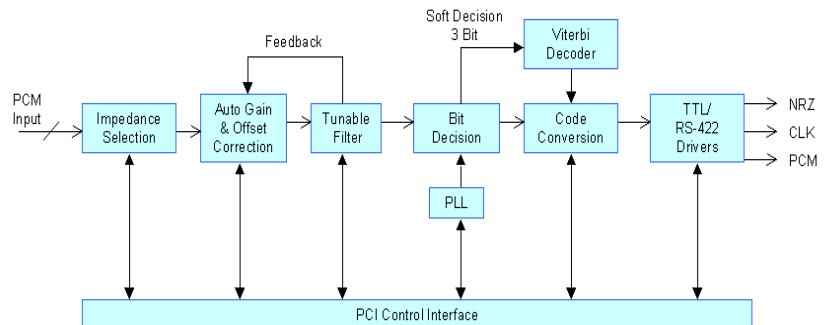
The PCM Bit Synchronizer card is a multifeatured, digitally-controlled bit synchronizer that provides state-of-the-art BER performance. The TSNC bit sync excels in harsh noise conditions with signal-to-noise capabilities superior to every other board and box level unit in its class.

The TSNC module represents a breakthrough in high-speed digital bit synchronizers. Its patented phase-lock loop and tracking features enable the TSNC bit sync to attain performance levels equal to box-level bit synchronizers costing two to three times as much.

Occupying a single PCI bus card slot, the TSNC bit sync provides complete front-end flexibility to the system integrator. Programmability includes selection of source and impedance, input code type and polarity, bit rate, loop and tracking bandwidths, output code, and clock phase.

An optional on-board convolutional (Viterbi) decoder provides programmable symbol inversion and symbol order, differential conversion, and descrambling. An on-board encoder is also provided. Optional (30,116) Interleaver/Deinterleaver supports Space Network Users Guide (SNUG) and Consultative Committee for Space Data System (CCSDS) specifications.

The TSNC bit sync is used in PCM applications where noise-reliable solutions are required for noise perturbation problems. Our bit sync design, which has received a U.S. patent, uses the low-power, high-reliability circuit components of today's technologically advanced markets. The automatic self-calibration of internal filters provides built-in adjustments over the lifetime of the board to offset the inevitable problems of component aging.



<b>Input Signal</b>	Codes	NRZ-L/M/S, BIØ-L/M/S, DBIØ-M/S, DM-M/S, MDM-M/S, RZ
	Level	250 mV to 10 volts peak-to-peak
	Derandomizer	Forward & reverse, 5 lengths; 9, 11, 15, 20, 23
	Impedance	75 ohms, or 10K ohms, 50 ohms available (RS-422 = 110 ohms)
	Sources & Type	Four external data inputs, single-ended or differential (RS-422–Source 4 only, jumper-select); only Source 4 with low power option
	Polarity	Normal or inverted (programmable)
	Loop Bandwidth	0.004% to 5% (programmable; 0.004% resolution)
<b>Performance</b>	Operating Range (NRZ codes)	10 bps to 20 Mbps; option to 40 Mbps
	Operating Range (All other codes)	10 bps to 10 Mbps; option to 20 Mbps
	Bit Error Rate	Within 1.0 dB of theoretical curve up to maximum data rate
	Acquisition Range	Up to +/- 5% of programmed data rate, $E_b/N_o = 15$ dB
	Acquisition Time	Within 50 bits, average, random data within 0.5% deviation from the programmed data rate, $E_b/N_o = 15$ dB
	Sync Maintenance	Retains sync with NRZ codes at $E_b/N_o = 3$ dB with 128 bit transition gaps occurring every 1024 bits with random data
	Bit Slippage	Maintains phase with BIØ codes at $E_b/N_o = 12$ dB with over 2000 continuous 1's or 0's, at $E_b/N_o = 0$ dB with random data (NRZ & BIØ)
<b>Output</b>	Tracking Range	Exceeds +/- 20% of programmed data rate
	Baseline Variation	No degradation beyond 1 dB from theoretical performance curve with super-imposed wave form equal to 100% of the peak-to-peak signal input at 0.1% of the bit rate, BIØ codes
	DC Offset	100% of input signal level up to +/-10 Volts
	NRZ-L Data	TTL compatible into 50 ohms, and RS-422 Differential, with 0° clock
	* Selectable Data (x2)	Programmable PCM, TTL compatible into 50 ohms, and RS-422
	* Selectable Clock (x2)	Programmable 0° and 180°, phase, TTL and RS-422 outputs
	* Selectable Data	+/-1V into 50 ohms
<b>Electrical and Environmental</b>	* Optional Decoder (Per CCSDS & SNUG)	Optional on-board decoder, Rate 1/2 and Rate 1/3, constraint length 7, accepts 3-bit soft-decision input (internal bit decision). Programmable symbol order and inversion and differential decoding
	* Optional Deinterleaver	Periodic deinterleaving (30,116) with SNUG cover sequence (per CCSDS & SNUG)
	Form Factor	Full length PCI card
	Temperature	0° to 50 °C (operating), -20 °C to 80 °C (storage)
	Humidity	20 to 95% noncondensing
	* Power	+5V @ 1.5 amps, +12V @ 0.480 amps, -12V @ 0.520 amps Low Power Option: +5@ 1.3A, +12V to 90 mA and -12V to 60 mA
	Status	Sync, input, amplitude, rate deviation via PCI bus
<b>Ordering Codes</b>	Connectors	D-type connectors on card edge
	Programming	Programming via PCI bus, 32-bit
	TSNCxx-400	PCI Bit Sync, xx = 20 or 40 (Mbps)
	TSNCxx-400-C03	PCI Bit Sync Option: Convolutional (Viterbi) Decoder
	TSNCxx-400-D03	PCI Bit Sync Option: Deinterleaver/Decoder
	* TSNCxx-400-LPx	Low Power PCI Bit Sync, xx = 20 or 40 (Mbps); excludes decoder options
	Accessories	Software
	Documentation	Technical Reference Manual; installation and program information

\* Items removed or modified. Contact our factory for details.

Note: Specifications do not apply for all possible combinations of bit sync settings and signal perturbations.