

PCI All-in-One Board with IRIG Time Upgrade PPCMxx-100T / PPCMxx-1xyT

Features

- **Bit Sync, Decom, Simulator, Time Reader**
- **Occupies Single PCI Card Slot**
- **Operation to 50 Mbps**
- **Accepts All IRIG PCM Codes**
- **Accepts IRIG A, B, and G Time Codes**
- **Supports IRIG Class II Decommutation**
- **1 dB Bit Sync Performance**
- **Optional Convolutional Decoder/Encoder**
- **Optional QPSK, UQPSK Support**



Introduction

The PCI All-in-One board combines advanced capabilities of the Bit Synchronizer, Decommutator, Simulator, and Time module into a single PCI slot. Stand-alone Windows loader/driver software comes with the board for users building custom systems. As an option, a complete software suite is available to support a complete system.

Bit Synchronizer Function

Multifunction, digital control provides state-of-the-art BER performance. The Bit Sync excels in harsh noise conditions with superior signal-to-noise capabilities. The patented phase-lock loop and tracking features enable the Bit Sync to attain the performance levels of box-level bit synchronizers with equal performance.

Programmability includes selection of source and impedance, input code type, derandomization, polarity, bit rate, loop and tracking bandwidths, and output code and clock phase. An optional on-board convolutional decoder provides programmable symbol inversion and symbol order, differential conversion, and descrambling. Programmable built-in test is also provided.

Decommutator and Time Code Translator Functions

Supports full IRIG Class II PCM decommutation via a direct connection to the high-speed PCI computer bus. The Decom accepts data and clock inputs either from the PCM Bit Synchronizer or, in bypass mode, directly from an external data and clock source. IRIG time code inputs are translated to digital time setups with a one microsecond resolution. Time stamps are provided for each PCM minor frame. PCM data, minor frame status, and time words are output via direct memory addressing (DMA) block transfers over the PCI bus.

Simulator Function

A variable rate on-board simulator resides on the All-in-One board. It can be initiated to support the self-test of decommutator functions alone or the self-tests of both Bit Synchronizer and Decommutator functions. The simulator function features support for multiple programmable fixed-rate simulations using predefined data content.

By occupying a single PCI bus card slot, the PCI All-in-One board provides remarkable flexibility for the systems integrator while not compromising performance.

Bit Sync Input	Codes	NRZ-L/M/S, BIØ-L/M/S, DM-M/S, MDM-M/S	
	Level	500 mV to 10V peak-to-peak	
	Derandomizer	Forward & reverse, in 5 lengths: 9, 11, 15, 20, 23	
	Impedance	75 ohms, or 10 Kohms (programmable), 50 ohms available (single-ended); 110 ohms (differential)	
	Sources & Type	One or two single-ended (version-dependent) and one differential, programmable	
	Polarity	Normal or inverted, programmable	
	Loop Bandwidth	0.004% to 5%, programmable, 0.004% resolution	
	Operating Range	30 bps to 30 Mbps, option to 50 Mbps, NRZ codes 30 bps to 15 Mbps, option to 30 Mbps, all non-NRZ codes	
	Optional Decoder ¹ (Per CCSDS & SNUG)	Optional on-board decoder, rate ½, constraint length 7, accepts 3-bit soft-decision input (internal bit decision); programmable symbol order, inversion and differential decoding	
	Sync Status	TTL logic line indicating Bit Sync status; on-board LED status of bit-sync lock and PCM signal presence	
	PSK ¹	Optional support for QPSK and UQPSK inputs and convolutional encoded QPSK and UQPSK inputs; supports QPSK permutations	
	Bit Sync Performance	Bit Error Rate	Within 1.0 dB of theoretical to maximum data rates ²
		Acquisition Range	UP to ± 5% of programmed data rate
		Acquisition Time	Within 50 bits, average, random data within 0.5% deviation from the programmed data rate, $E_b/N_o = 15$ dB
		Sync Maintenance	Retains sync at $E_b/N_o = 3$ dB for NRZ at 50% transition density
Bit Slippage		Maintains phase with BIØ codes at $E_b/N_o = 12$ dB with over 2000 continuous ones or zeroes and at $E_b/N_o = 0$ dB for random data	
Tracking Range		± 20% of programmed data rate	
Baseline Variation		No degradation beyond 1 dB from theoretical performance curve with a superimposed wave form equal to 100% of the peak-to-peak signal input at 0.1% of the bit rate, BIØ codes	
DC Offset		DC offset plus peak signal plus noise ≤ 10V	
Loop Bandwidth		Continuously programmable with 0.02% resolution from 0.02 to 5.00%.	
Bit Sync Output		Data	NRZ-L, TTL-compatible into 50 ohms
	Clock	0° or 180°, programmable, TTL-compatible into 50 ohms	
	Tape ¹	Programmable PCM code, 1V peak-to-peak	
	Selectable Data ¹	Programmable PCM code, TTL compatible into 50 ohms	
	Selectable Clock ¹	Programmable 0° and 180°, phase, TTL	
Decom Input	Data & Clock	Internal NRZ-L data clock interface with Bit Sync (TTL) External NRZ-L data clock interface to by-pass Bit Sync (TTL)	
	Data Polarity	Auto, normal and inverse, programmable	
	Clock Phase	0° or 180°, programmable	
	Rate	10 bps to 30 Mbps, option to 50 Mbps	

Time Input	Time Input Source	External or internal, programmable
	External Time	IRIG A, B, G modulated carrier input; ¼, ½, 1, 2, 4 x rate, programmable; LED indicator of signal presence. Signal level 1.5 to 10V peak-to-peak from mark; 3-1 nominal (mark to space relationship)
	Internal Time	On-board timer seeded from any source internal to computer; e.g., computer clock, GPS receiver, etc.
Input to CVSD³ Card (-104 and -105 boards only)	Clock and Data Effective CVSD Data Rate	Serial clock and data supplied by the Decom 10 kbps to 40 kbps programmable data rate
	CVSD Word Density	Up to 50% CVSD word density in PCM stream
	Word Spacing	CVSD words must be equally spaced in the frame
	PCM Data Rate	32 kbps to 50 Mbps
	Companding	Three-bit companding
	Subword	Ability to extract 16-bit CVSD words out of data words. CVSD word will be the lower 16 bits
Output from CVSD Card³ (-104 and -105 boards only)	Audio Output	Differential and single-ended output signals for Audio hookup
	Selectable Gain	Normal Medium High
	Power output	Three outputs: <ul style="list-style-type: none"> ▪ 2W differential, amplified output available at external connector ▪ One line level output available at external connector ▪ One line level output available for internal connection to a sound board
Decom Processing	Sync Pattern Length ⁴	8 to 64 bits; programmable
	Sync Pattern Errors	0 to 16 bits; programmable
	Sync Word Mask	Any bits masked; programmable
	Sync Strategy	1 to 16 pattern matches (lock and drop); programmable
	Sync Modes	Normal and shift-register mode
	Bit Slip	0, ±1, ±2, ±3 bits; programmable
	Data Word Length	4 to 32 bits, programmable
	Orientation	MSB/LSB orientation, programmable
	Commutation	Super-, sub-, irregular; programmable
	Time	Independent time tag of each minor frame and each PCM input
	Minor Frame Length	Up to 65,536 words/minor frame; programmable
	Major Frame	Subframe decommutation handled by computer processor
	Major Frame Length ⁵	33,554,432 bits maximum major frame size. Up to 4096 minor frame/major frame; programmable
	Major Frame Sync ⁵	SFID, FCC, URC, or unique frame sync
	SFID ID Word ⁵	1 to 16 bits; programmable
	SFID Counter ⁵	Any word within minor frame; programmable
Direction/Start ⁵	Up or down, 0 or 1; programmable	
Frame Format Indent ⁵	Any word within minor frame; programmable; up to 16 different formats supported	

Decom Output	PCI Bus	32-bit transfers; 33 MHz +5V bus
	Sync Status	TTL logic line (w/ground) indicating status of decom; on-board status LEDs: minor frame lock, clock presence
Simulator Output	Data Clock	NRZ-L and 0° Clock, programmable input to Bit Synchronizer or decommutator
	Rate	Multiple programmable fixed-rate simulation
	Source	Multiple programmable formats; predefined data content
Time Output	Time Code Rate	Loop back of time input; signal properties of Time Code Out are virtually identical to the Time Code In
	Time Code & Level	Same as external time input
	Sync Status	On-board LEDs: IRIG time present/not present, decoding, and lock
Electrical and Environmental	Form Factor	Full-length, PCI-based module; universal slot compatibility
	Temperature	0° to 50 °C (operating), -20° to 80 °C (storage)
	Humidity	20 to 95% noncondensing
	Power	+5V @ 3.0A, +12V @ 175 mA, -12V @ 100 mA
	Status	Sync, input, amplitude, rate deviation via PCI bus
	Connectors	D-type connectors on card edge
	Programming	Programming via PCI bus, 32-bit

¹ Version-dependant, must be specified at time of order, requires a PCI Advanced All-in-One board.

² PPCMxx-100T provides 1 dB performance to 30 Mbps; 2 dB performance to 50 Mbps (with option).

PPCMxx-1xyT provides 1 dB performance to 30 Mbps; 1dB performance to 50 Mbps (with option).

³ Design conforms to IRIG Standard Chapter 5, "Digitized Audio Telemetry Standard."

⁴ With CVSD card (-104 and -105 boards) supported, sync pattern length is 8 to 32 bits, programmable.

⁵ Requires set-up software.

Note: Specifications do not apply to all possible combinations of Bit Synchronizer settings and signal perturbations.

Ordering Codes	PPCMxx-100T-ab2	PCI All-in-One PCM Board with IRIG Time Upgrade; Mbps: xx = 30 or 50 Mbps, ab = available options, which are detailed below
	PPCMxx-1xyT-ab3	PCI Advanced All-in-One PCM Board with IRIG Time Upgrade; Mbps: xx = 30 or 50 Mbps, ab = available options, detailed below
	xy Options – QPSK,	x = 0, FM/BPSK only; M, QPSK Master; or S, QPSK Slave
	Convolutional Decoder	y = 0, no option; or C, Convolutional Decoder option
	ab Options – I/O:	
	PPCMxx-XXXX-VXX	RS-422 Embedded Output
	PPCMxx-XXXX-XCX	CVSD (Voice Option) Upgrade to All-in-One Board
	PPCMxx-XXXX-XEX	ECL Input Interface
	PPCMxx-XXXX-XSX	TTL Embedded Output
	Accessories	Software
Cable		D-type to BNC cable assembly included with board
Documentation		Technical reference manual; installation and programming information