

VME PCM Bit Synchronizer Board VSNCxx-70x

Features

- Tunable Bit Rates Up to 40 Mbps
- Occupies Single VME Slot
- Selectable IRIG PCM Formats
- Selectable Loop Bandwidths
- BER Performance Better than 1.0 dB
- Complete Programming Documentation and Stand-alone Setup Software
- Optional Convolutional (Viterbi) Decoder and Deinterleaver
- Built-in Self-test Pattern Generator
- Optional Support for QPSK PCM Streams
- Optional On-board Decommutator and Simulator



Introduction

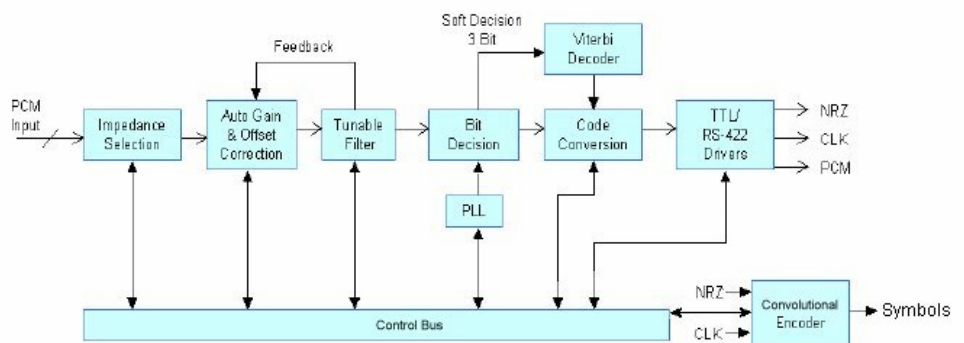
The PCM Bit Synchronizer card is a multifeatured, digitally controlled bit synchronizer, which provides state-of-the-art BER performance. The VSNC bit sync excels in harsh noise conditions with signal-to-noise capabilities superior to every other board and box level unit in its class.

The VSNC module represents a breakthrough in high-speed digital bit synchronizers. Its patented phase-lock loop and tracking features allow the VSNC bit sync to attain the performance levels of box-level bit synchronizers costing two to three times as much with equal performance.

Occupying a single VME bus card slot, the VSNC bit sync provides complete front-end flexibility to the system integrator. Programmability includes selection of source and impedance, input code type and polarity, bit rate, loop and tracking bandwidths, output code and clock phase.

An optional on-board convolutional (Viterbi) decoder provides programmable symbol inversion and symbol order, differential conversion, and descrambling. An on-board encoder is also provided. Optional (30,116) Interleaver/ Deinterleaver supports Space Network Users Guide (SNUG) and Consultative Committee for Space Data System (CCSDS) specifications.

The VSNC bit sync is used in PCM applications where noise-reliable solutions are required for noise perturbation problems. Our bit sync design, which has received a U.S. patent, uses the advanced, low-power, high-reliability circuit components available on the market today. The automatic self-calibration of internal filters provides built-in adjustments over the lifetime of the board to offset the inevitable problems of component aging.



Input Signal	Codes	NRZ-L/M/S, BIØ-L/M/S, DBIØ-M/S, DM-M/S, MDM-M/S, RZ
	Level	250 mV to 10 volts peak-to-peak
	Derandomizer	Forward & reverse, 5 lengths; 9, 11, 15, 20, 23
	Impedance	75Ω, 10K ohms, and 50 ohms available
	Sources & Type	Four external data inputs, single-ended or differential (RS-422 - source 4 with jumpers)
	Polarity	Normal or inverted (programmable)
	Loop Bandwidth	0.004% to 5% (programmable, 0.004% resolution)
	Operating Range	NRZ: 10 bps to 5 Mbps; options to 40 Mbps All others: 10 bps to 2.5 Mbps; options to 20 Mbps
Performance	Bit Error Rate	Within 1.0 dB of theoretical curve up to maximum data rate
	Acquisition Range	Up to +/- 5% of programmed data rate, $E_b/N_o = 15$ dB
	Acquisition Time	Within 50 bits, average, random data within 0.5% deviation from the programmed data rate, $E_b/N_o = 15$ dB
	Sync Maintenance	Retains sync with NRZ codes at $E_b/N_o = 3$ dB with 128 bit transition gaps occurring every 512 bits with random data
	Bit Slippage	Maintains phase with BIØ codes at $E_b/N_o = 12$ dB with over 2000 continuous 1's or 0's at $E_b/N_o = 0$ dB with random NRZ & BIØ data
	Tracking Range	Exceeds +/- 20% of programmed data rate
	Baseline Variation	No degradation beyond 1 dB from theoretical performance curve with superimposed wave form equal to 100% of the P-P signal input at 0.1% of the bit rate, BIØ codes
	DC Offset	100% of input signal level up to +/-10 Volts
Output	NRZ-L Data	TTL compatible into 50 ohms and RS-422 Differential with 0° clock
	Selectable Data (x2)	Programmable PCM, TTL compatible into 50 ohms and RS-422
	Selectable Clock (x2)	Programmable 0° and 180°, phase, TTL and RS-422 outputs
	Selectable Data	+/-1V into 50 ohms
	Optional Decoder (Per CCSDS & SNUG)	Optional on-board decoder, Rate $1/2$ and Rate $1/3$, constraint length 7, accepts 3-bit soft-decision input (internal bit decision). Programmable symbol order, inversion, and differential decoding
	Optional Encoder	Independent Data/Clock input 10 symbols/second to 20 Million symbols/second output
	Optional Deinterleaver	Periodic deinterleaving (30,116) with SNUG cover sequence (per CCSDS & SNUG)
	Electrical and Environmental	Form Factor
Temperature		0 °C to 50 °C (operating), -20 °C to 80 °C (storage)
Humidity		20 to 95% noncondensing
Power		+5V @ 1.30 amps, +/- 12V @ 0.30 amps
Status		Sync, input, amplitude, rate deviation via VME bus
Connectors		D-type connectors on card edge
Programming		Programming via VME bus, 32-bit
Ordering Codes	VSNCxx-70x-abc	VME-based PCM Bit Sync, xx = 20 or 40 (Mbps)
	VSNCxx-x1x-abc	VME Bit Sync Option: Convolutional (Viterbi) Decoder and Encoder
	VSNCxx-x2x-abc	VME Bit Sync Option: Deinterleaver/Decoder
Accessories	Documentation	Technical Reference Manual; installation and programming info.

Note: Specifications do not apply for all possible combinations of bit sync settings and signal perturbations.