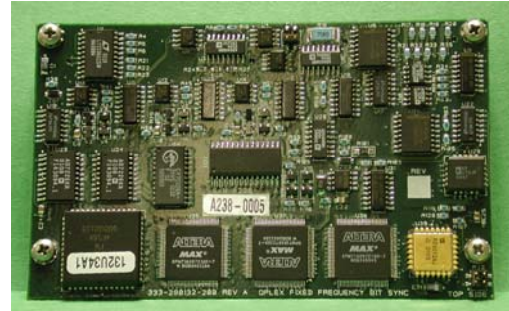


## Quadraplex PCM Bit Synchronizer Board QSNCyyyyK-LCT-1

### Features

- Fixed Bit Rates Up to 30 Mbps, All Codes!
- Occupies Single Daughter Card Location
- Up to Four Bit Syncs Per VME Slot
- Selectable IRIG PCM Formats
- Selectable Loop Bandwidths
- Selectable Input Impedance of 50, 75, and 10K ohms
- BER Performance Better than 1.0 dB
- Output Status LED Drivers



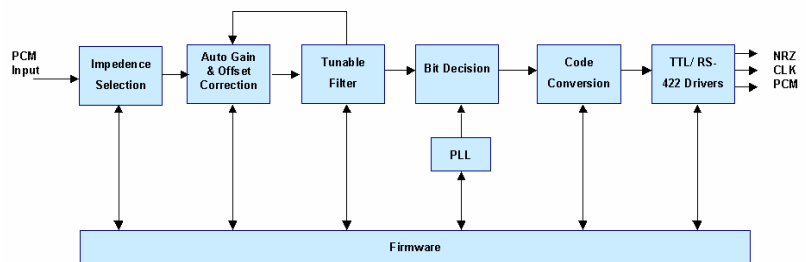
### Introduction

The PCM Bit Synchronizer card is a multifeatured, digitally controlled bit synchronizer that provides state-of-the-art BER performance. The QSNC bit sync excels in harsh noise conditions with signal-to-noise capabilities superior to every other board and box level unit in its class.

The QSNC module represents a breakthrough in high-speed digital bit synchronizers. Its patented phase-lock loop and tracking features allow the QSNC bit sync to attain the performance levels of box-level bit synchronizers costing two to three times as much with equal performance.

Occupying a single VME quadraplex daughter card position, the QSNC bit sync provides complete front-end flexibility to the system integrator. Full-time selectability includes impedance and polarity, while programmability at the time of order includes input code type, bit rate, and loop bandwidth.

The QSNC bit sync is used in PCM applications where noise-reliable solutions are required for noise perturbation problems, and where highly compact PCM bit synchronization hardware is essential. Our bit sync design, which has received a U.S. patent, uses the most advanced, low-power, high-reliability circuit components available on the market today. The automatic self-calibration of internal filters provides built-in adjustments over the lifetime of the board to offset the inevitable problems of component aging.



<b>Input Signal</b>	Codes	NRZ-L/M/S, BIØ-L/M/S, DBIØ-M/S, DM-M/S, MDM-M/S, RZ
	Level	500 mV to 10 volts peak-to-peak
	Derandomizer	5 lengths; 9, 11, 15, 20, and 23
	Impedance	50 ohms, 75 ohms (default), and 10K ohms (hardware programmable)
	Sources & Type	One external data input, single-ended or differential (RS-422 levels)
	Polarity	Normal or inverted (hardware programmable)
	Loop Bandwidth	0.05% to 5% (programmable at time of ordering – see ordering notes)
	Operating Range (NRZ codes)	10 bps to 30 Mbps
	Operating Range (All other codes)	10 bps to 30 Mbps
	<b>Performance</b>	Bit Error Rate
Acquisition Range		Up to +/- 5% of programmed data rate (limited by configuration)
Acquisition Time		Within 50 bits, average, random data within 0.5% deviation from the programmed data rate, $E_b/N_o = 15$ dB
Sync Maintenance		Retains sync with NRZ codes at $E_b/N_o = 3$ dB with 128-bit transition gaps occurring every 512 bits with random data
Bit Slippage		Maintains phase with BIØ codes at $E^b/N^o = 12$ dB with over 2000 continuous 1's or 0's, at $E^b/N^o = 0$ db with random data (NRZ & BIØ)
Tracking Range		Up to +/- 20% of programmed data rate (limited by configuration)
Baseline Variation		No degradation beyond 1 dB theoretical performance curve with superimposed wave form equal to 100% of the peak-to-peak signal input at 0.1% of the bit rate, BIØ codes
DC Offset		100% of input signal level up to +/-10 Volts
<b>Output</b>	NRZ-L Data	TTL compatible into 50Ω and RS-422 Differential
	Clock	Selectable 0° and 180° phase; TTL or RS-422 output
<b>Electrical and Environmental</b>	Form Factor	Single-slot, Quadraplex Form Factor
	Temperature	0 °C to 50 °C (operating), -20 °C to 80 °C (storage)
	Humidity	20 to 95% noncondensing
	Power	+5V @ 1.30 amps, +/- 12V @ 0.30 amps
	Status	Sync status via discrete logic
	Connectors	D-type connectors on carrier card
<b>Accessories</b>	Documentation	Technical Reference Manual; installation and program information
	Carrier Card	QPLX-324-01

**Ordering Codes**      QSNCyyyyK-LCT-x      Quadrplex-based PCM Bit Sync

Where:    yyyy = bit rate, from 0010 to 3000

          K = number of zeros for bit rate

Examples: 30 Mbps = 30,000,000 bps = 3000 x10<sup>4</sup> = QSNC3004

          3000 is the “yyyy” and the exponent of 4 (for 4 additional zeros) for K

          10 bps = 10 bps = 0010 x10<sup>0</sup> = QSNC00100

          0010 is the “yyyy” and the exponent of 0 (for no additional zeros) for K

Decimal points are supported for bit rates from 10 bps to 99 bps with the use of R as the decimal place (note that K will always be zero). Thus, 14.3 bps = 14.3 bps = 14R3 x10<sup>0</sup> = QSNC14R30

          0010 is the “yyyy” and the exponent of 0 (for no additional zeros) for K

**L = Loop Widths**

Examples:	0	0.05%	G	1.60%
	1	0.10%	H	1.70%
	2	0.20%	J	1.80%
	3	0.30%	K	1.90%
	4	0.40%	L	2.00%
	5	0.50%	M	2.20%
	6	0.60%	N	2.40%
	7	0.70%	P	2.60%
	8	0.80%	R	2.80%
	9	0.90%	S	3.00%
	A	1.00%	T	3.20%
	B	1.10%	V	3.40%
	C	1.20%	W	3.70%
	D	1.30%	X	4.00%
	E	1.40%	Y	4.50%
	F	1.50%	Z	5.00%

Note: U indicates a unique configuration by the user

**C = Input Code**

Examples:	0	NRZ-L	5	BIØ -S	A	RNRZ-L, (2 <sup>-11</sup> )-1
	1	NRZ-M	6	DM-M	B	RNRZ-L, (2 <sup>-15</sup> )-1
	2	NRZ-S	7	DM-S	C	RNRZ-L, (2 <sup>-20</sup> )-1
	3	BIØ -L	8	M <sup>2</sup>	D	RNRZ-L, (2 <sup>-23</sup> )-1
	4	BIØ -M	9	RZ		

T = Tracking Loops	Numbers are "times loop width" from variable "L"	
Examples:	0	1½ times
	1	2 times
	2	2½ times
	3	3 times
	4	4 times
	5	5 times
	6	10 times

Note: U indicates a unique configuration by the user.

X = Hardware Version

**Unit Examples:** QSNC11523-300-1 is a unit that accepts an NRZ-L input code at 1.152 Mbps, a loop bandwidth of .3%, and a tracking bandwidth of .45%.

QSNC85R3-XD5-1 is a unit that accepts an RNRZ-L, (2<sup>-23</sup>)-1 input code at 85.3 bps and has a loop bandwidth of 4.0% with a tracking range of 20%.

*Note: Specifications do not apply for all possible combinations of bit sync settings and signal perturbations.*