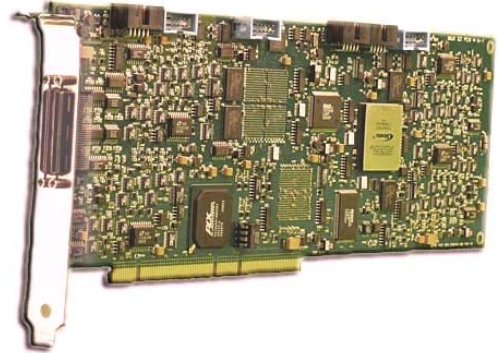


PCI Four-Channel All-in-One Board with IRIG Time Upgrade PPCMxx-30xT

Features

- 1 to 4-Channel Bit Sync, Decom, Simulator, Time Reader
- Occupies Single PCI Card Slot
- Operation to 60 Mbps
- Accepts All IRIG PCM Codes
- Accepts IRIG A, B, and G Time Codes
- Supports IRIG Class II Decommutation
- 1 dB Bit Sync Performance
- Convolutional Decoder/Encoder
- Supports QPSK Permutation



Introduction

The Four-channel PCI All-in-One board can combine the advanced capabilities of the Bit Synchronizer, Decommutator, Simulator, and Time module into a single PCI slot. A wide variety of board configurations are available to support applications ranging from Bit Sync only requirements to complete ground station capability for multiple PCM streams. Stand-alone Windows loader/driver software comes with the board for users requiring custom systems. As an option, a complete software suite is available to provide comprehensive ground station capabilities.

Bit Synchronizer Function

Multi-feature, digital control provides state-of-the-art BER performance. The Bit Sync excels in harsh noise conditions with superior signal-to-noise capabilities. The patented phase-lock loop and tracking features enable the Bit Sync to attain the performance levels of box-level Bit Synchronizers with equal performance.

Programmability includes selection of source and impedance, input code type, derandomization, polarity, bit rate, loop and tracking bandwidths, and output code and clock phase. An optional on-board convolutional decoder provides programmable symbol inversion and symbol order, differential conversion, and descrambling. Programmable built-in test (BIT) is also provided with integrated Bit Error Rate Test (BERT) capability.

Decommutator and Time Code Translator Functions

The PPCMxx-30xT supports full IRIG Class II PCM decommutation via a direct connection to the high-speed PCI computer bus. The Decom accepts data and clock inputs either from the PCM Bit Synchronizer or, when in bypass mode, directly from an external data and clock source. IRIG time code inputs are translated to digital time setups with a one microsecond resolution. Time stamps are provided for each PCM minor frame.

PCM data, minor frame status, and time words are output via direct memory addressing (DMA) block transfers over the PCI bus.

Simulator Function

A variable rate, on-board simulator resides on the All-in-One board. It can be programmed to support the self-test of decommutator functions alone or the self-tests of both Bit Synchronizer and Decommutator functions. The programmable simulator can also be used to exercise software functionality.

By occupying a single PCI bus card slot, the PCI All-in-One board provides remarkable flexibility for the systems integrator while not compromising performance.

Bit Sync Input	Channels	2 or 4, independent data synchronization & clock generation channels
	Programmability	Each Bit Sync input channel independently programmed
	Codes	NRZ-L/M/S, BIØ-L/M/S, DM-M/S, MDM-M/S
	Level	300 mV to 10V peak-to-peak
	Sources & Type	One single-ended & one differential per channel, programmable
	Impedance	50 ohms, 75 ohms, or 10 Kohms (single-ended), programmable; 110 ohms (differential)
	Derandomizer	Forward & reverse, in 5 lengths: 9, 11, 15, 20, 23, programmable
	Polarity	Normal or inverted, programmable
	Operating Range (extended range available)	30 bps to 30 Mbps, option to 60 Mbps, NRZ codes 30 bps to 15 Mbps, option to 30 Mbps, all non-NRZ codes
Sync Status	TTL logic line indicating Bit Sync status; on-board LED status of Bit-Sync lock & PCM signal presence	
Decoder (Optional)	Convolutional Decoder (Per CCSDS & SNUG) Viterbi Decoding	Rate 1/2 , constraint length 7, coefficients 133 & 171; accepts 3-bit soft-decision input (internal bit decision); programmable symbol order, inversion & differential decoding
	Re-sequencer for QPSK	Optional support for BPSK, QPSK & OQPSK inputs & convolutional encoded QPSK & OQPSK inputs; supports QPSK permutations
	De-Interleaving	Programmable periodic convolutional de-interleaving & interleaving
Bit Sync Performance	Bit Error Rate	Within 1.0 dB of theoretical to maximum data rates
	Baseline Variation	No degradation beyond 1 dB from theoretical performance curve with a superimposed wave form equal to 100% of the peak-to-peak signal input at 0.1% of the bit rate, BIØ codes
	Acquisition Range	Up to $\pm 5\%$ of programmed data rate
	Acquisition Time	Within 50 bits, average, random data within 0.5% deviation from the programmed data rate, $E_b/N_o = 15$ dB
	Loop Bandwidth	0.02% to 5%, programmable, 0.02% resolution
	Tracking Range	$\pm 20\%$ of programmed data rate
	Sync Maintenance	Retains sync at $E_b/N_o = 3$ dB for NRZ at 50% transition density
	Bit Slippage	Maintains phase with BIØ codes at $E_b/N_o = 12$ dB with over 2000 continuous ones or zeroes & at $E_b/N_o = 0$ dB for random data
	DC Offset	DC offset plus peak signal plus noise $\leq 10V$
Optional	E_b/N_o Measurement	Detect & generate indication of signal input E_b/N_o , ranging from < 0.0 dB to >15.0 dB with 0.1 dB resolution, accurate to within 0.5 dB of true SNR
	BERT	BER count report over PCI bus

Bit Sync Output	Data	Programmable PCM output codes (same as input codes); TTL-compatible into 50 ohms
	Clock	0°, fixed, TTL-compatible into 50 ohms 0°, 90°, 180°, 270°, programmable, TTL-compatible into 50 ohms 2X frequency, TTL-compatible into 50 ohms
	Optional	QPSK data (recombined) & 0° clock output, TTL-compatible into 50 ohms
Optional	Additional Outputs (per channel)	All TTL capable of driving 50 ohms RS-422 & additional TTL NRZ-L data & 0° clock RS-422 & TTL, programmable PCM code TTL, 3-bit soft decision outputs
Optional	Independent Convolutional Encoder	Independent Convolutional Encoder data & clock inputs (TTL) and Convolutional Encoder data outputs Auto detect clock presence (100K to 10M); if not present, will generate PN15 pattern as Encoder input
Optional	E_b/N_o	Capable of supporting remote panel E_b/N_o display & output over remote control interface
	BERT Pattern	Capable of independent generation of pseudorandom BERT pattern, max length +15
	BERT PCM Codes	All PCM codes supported by Bit Sync input
	BERT Levels	TTL-compatible into 50 ohms
	BERT Clock	TTL, 0° (fixed)
Optional	BDS Data	Best data selection of PCM inputs comprising board assembly (from 2, 3, or 4 Bit Sync modules); generates BDS NRZ-L output
Optional	BDS Clock	TTL, 0° clock (fixed); no additional clock cycles occur during BDS switch
Control	PCI Bus	PCI-66 MHz, 64-bit interface
	Optional	Serial control interface, RS-232 or RS-485
Decom Input (optional)	Data & Clock	Internal NRZ-L data clock interface with Bit Sync (TTL) External NRZ-L data clock interface to by-pass Bit Sync (TTL)
	Data Polarity	Auto, normal & inverse, programmable
	Clock Phase	0° or 180°, programmable
	Rate	10 bps to 30 Mbps, option to 50 Mbps
	Processing	Full IRIG Class II PCM programmable decommutation
Time Input (optional)	Number of Channels	One independent time channel
	Programmability	Time channel programmed independently
	Time Input Source	External or internal, programmable
	Level	Signal level 0.5 to 10 Vp-p from mark, 3-1 nominal, mark-to-space relationship
	Impedance	10 Kohm
	Code	IRIG A, B, G modulated carrier input
	Internal Time	On-board timer seeded from any source internal to computer; e.g., computer clock, GPS receiver, etc.

Simulator Output (optional)	Data Clock	NRZ-L & 0° clock, programmable input to Bit Synchronizer or Decommutator
	Rate	Multiple programmable rate simulation
	Source	Multiple programmable formats, predefined data content
Electrical & Environmental	Form Factor	Full-length, PCI-based module; universal slot compatibility PCI-66 MHz, 64-bit based module
	Temperature	0° to 50 °C (operating), -20° to 80 °C (storage)
	Humidity	20 to 95% noncondensing
	Power	12W typical, +3.3V at 3.4A
	Status	Bit Sync: bit lock, input amplitude , rate deviation via PCI bus Decom: frame & minor frame lock Time: signal lock
	Connectors	AMP 748394-1 connectors on card edge
	Programming	Programming via PCI bus, 64-bit
Software	Loader / Driver	Complete loader/driver software included with board to support customer development (sample source code provided) Factory assistance available
	Data handling	Comprehensive software suite available for data processing, distribution & display. Includes board programming.