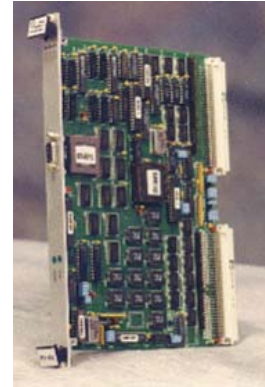


VME/GME SCSI Bridge Interface BDG-326

Features

- High-speed RIO/VME Data Routing
- Dual-speed Options Available
- Built-in Self-test and Data Monitoring

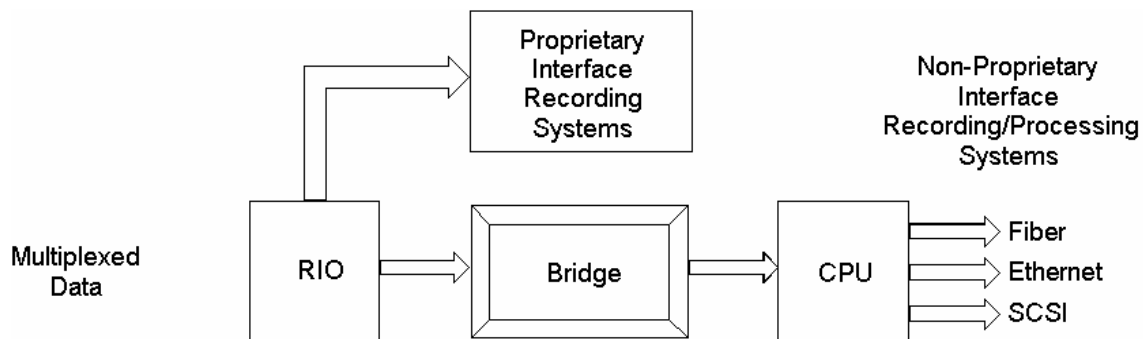


Introduction

The VME/GME SCSI Bridge Interface design provides a link between the Recorder I/O (RIO), DCRsi, or DIS recorder to the VME bus. The board is capable of being a slave-only interface to the VME bus for 32-bit data access, 32-bit block transfer access, or 64-bit block transfer access. Additionally, the board can operate as a bus master under all three data-transfer modes by maintaining a circular buffer in the VME addressing space. Slave mode or master mode is programmable via the VME bus and requires VME setup and control.

This design includes the capability to emulate a DCRsi-type recorder. In this mode, the board accepts data from external sources in record and plays the data out in playback. The board can also act as a peripheral connected to a DCRsi or equivalent-type recorder. In this mode, the interface provides data to the recorder in the record mode and accepts data from a recorder in playback mode. The two modes of operation are supported with jumpers.

The bridge operates as an interface between an 8-bit wide ECL parallel interface and the VME bus. It contains a 4K x 32 bidirectional FIFO segment, which is directly accessed by the 8-bit wide parallel interface as well as the VME bus. The FIFO contains programmable “almost empty” and “almost full” flags, which are used to initiate VME access to the FIFO. By using these flags each time, a VME access is initiated and a known quantity of data is available for transfer without any additional overhead associated with checking the status of the FIFO. In record mode, the “almost empty” flag indicates that there is at least this much data ready to be moved. In playback mode, the “almost full” flag indicates that there is at least this much room in the FIFO for additional data.



The VME bus arbitrator arbitrates the bus based on the FIFO status flags. In block transfer mode, 256 bytes are transferred each time the bus is granted. Per the VME bus specification, nothing short of a VME bus error will terminate a block transfer prematurely. In programmed data mode, the system performs a complete 256-byte transfer, provided that the bus-clear or bus-error signals are not asserted. The programmed data mode asserts a new address prior to each cycle unlike the block transfer mechanism.

The VME bus interrupter provides software control over the interrupt vector (8-bit vector fetch), as well as overall interrupt enable/disable control. There is an interrupt source mask to individually select/deselect interrupt sources; this selection is left to the software programmer.

When operating as a slave-only interface on the VME bus, the board is capable of handling block transfers of 32-bit and 64-bit width. The 32-bit transfer is a single-wait state access, and the 64-bit transfer is a two-wait state access. The slave-only block transfer interface uses an interrupt to indicate when either enough data or enough room is available in the FIFOs. This ensures that a complete transfer can occur without the risk of under- or overflowing the FIFOs.

Data Input	8-bit ECL, DCRsi Emulation	
Transfer Modes	Block Transfer, Programmed Data	
Operational Modes	Master, Slave	
Data Flags	FIFO Empty, Almost Empty, Almost Full, Full	
VME Addressing	A32	
VME Bus Speed	16 MHz	
Internal Bus Speed	24 MHz	
Bus Interfaces	VME; GME	
Built-in Test	VME Registers, VME Bus Operation, VME Interrupter	
Front Panel Status	LEDs for Bus Master, Data Ready, +5V, -5.2V	
Status Register	Underflow, Overflow, Block Transfer Complete, Test Mode, Block Ready, Bus Error	
Electrical/Environment	Form Factor	IMUX Quadraplex submodule
	Connectors	Motherboard I/O
	Indicators	Channel active and FIFO overflow
	Operating Temperature	32 to 158 °F (0 to 70 °C)
	Storage Temperature	14 to 185 °F (-10 to 85 °C)
	Operating Altitude	0 to 10,000 feet (0 to 3,000 meters)
	Storage Altitude	-1,000 to 20,000 feet (-300 to 6,200 meters)
	Humidity	20 to 95% noncondensing